REMARKS

This application has been carefully reviewed in light of the Office Action dated October 23, 2003. Claims 87-90 have been amended. Claims 97-99 have been added. Claims 87-99 are now pending. Applicant reserves the right to pursue the original claims and other claims in this and other applications. Applicant respectfully requests reconsideration of the above-referenced application in light of the foregoing amendments and following remarks.

Claims 87-88 and 90-96 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakagawa in view of Tracy. The rejection is respectfully traversed and reconsideration is requested.

Nakagawa does not teach or suggest "forming a substrate; forming a layer of magnetic field shielding material over said substrate; forming an insulating layer over said layer of magnetic field shielding material; providing a support surface for an integrated circuit chip, said substrate, layer of magnetic field shielding material, insulating layer and support surface forming part of a chip carrier; and supporting an integrated circuit chip with said chip carrier, said chip carrier having a top and bottom surface." as recited in claim 87 (emphasis added).

Nakagawa is directed toward the manufacture of a printed circuit board (Col. 6, lines 24-25) and not a chip carrier as Applicant's claim. In FIG. 1 of Nakagawa, a "printed circuit board 10" is illustrated (Col. 4, lines 15-17). In contrast, in Applicant's FIG. 6, a printed circuit board 400 is illustrated electrically connected to a chip carrier through solder balls 280. Applicant's claimed chip carrier comprises substrate 120, a magnetic field shielding layer 113 formed over the substrate 120, and an insulating layer 140 formed over the magnetic field shielding layer 113. All of which is illustrated in Applicant's FIG. 6.

Accordingly, as noted, Nakagawa does not teach or suggest Applicant's claimed chip carrier for supporting an integrated circuit chip having a substrate, a layer of magnetic

field shielding material formed over the substrate, and an insulating layer formed over the layer of magnetic field shielding material.

Tracy is relied upon for teaching at least one layer of magnetic field shielding material in contact which a chip (Office Action, pg. 3); but, does not teach a method of forming a chip carrier, as recited in claim 87. Tracy teaches a "non-volatile magneto-resistive memory positioned on a substrate and a passivation layer at least partially surrounding the non-volatile magneto-resistive memory." (Col. 2, lines 18-21). Tracy's "passivation layer includes ferrite materials for shielding the non-volatile magneto-resistive memory from stray magnetic fields." (Col. 2, lines 21-23).

However, Tracy's structure is completely different from Applicant's claimed chip carrier. Tracy discloses a structure that "has a plurality of magnetic layers including a first magnetic layer 11 and a second magnetic layer 13 . . . [which] are separated by a first conductive spacer 12." (Col. 2, lines 62-64). Then, the passivation layer 18 is formed either on the "the surface of cell 10 or a thin layer 17 of dielectric material." (Col. 5, lines 5-7).

Neither of the cited references teach a method of forming Applicant's claimed chip carrier. In addition, Tracy teaches forming a passivation layer on top of the memory cell 10. Tracy does not teach forming a magnetic field shield layer between the substrate and insulating layer. For at least these reasons, the prior art of record does not teach or suggest the features found in claim 87.

Moreover, in Col. 18, Nakagawa teaches "the results of the experiments conducted by the inventors et al. show that these layers [i.e, el. 22] may be formed on only one of the surfaces of the base plate 12," (Col. 18, lines 13-15) (emphasis added). Thus, Nakagawa teaches that the copper ink layer 22' should be provided on one side of the base plate 12 and not to both a top and bottom surface.

Accordingly, the prior art of record does not teach or suggest a method of forming the recited chip carrier. Similarly, the cited references do not teach of suggest "providing a second layer of magnetic field shielding material on top of said chip carrier," as recited in claim 88 (emphasis added), or "providing a second layer of magnetic field shielding material embedded within a printed circuit board electrically coupled to said chip carrier," as recited in claim 90 (emphasis added).

Claims 88 and 90-96 depend from claim 87 and are allowable for at least the reasons set forth above with regard to independent claim 87. Withdrawal of the § 103(a) rejection is respectfully solicited.

Claim 89 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakagawa in view of Tracy and further in view of Lin. The rejection is respectfully traversed and reconsideration is requested.

Claim 89 depends from claim 87 and is similarly allowable for at least the reasons presented above with regard to claim 87. Lin is relied upon for teaching a second layer of magnetic field shielding material embedded within the substrate and does not rectify the deficiencies associated with Nakagawa and Tracy. For at least these reasons, claim 89 should be allowable over the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant